VOICE TRANSMISSION AT 6000 BITS PER SECOND USING DELTA MODULATION

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THESIS

VOICE TRANSMISSION AT 6000 BITS PER SECOND USING DELTA MODULATION

by

Elias Emmanuel Padouvas

December 1979

Thesis Advisor: G. Myers

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Digital systems are of major importance in modern communications. This research investigates the minimum clock (bit) rate of a commercially available delta modulator/demodulator needed to transmit intelligible voice signals.

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#20 - ABSTRACT - CONTINUED

Intelligible voice and music signals were recovered using a clock rate as low as 6 Kbits/sec.

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Voice Transmission at 6000 Bits Per Second Using Delta Modulation

by

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Lieutenant, Hellenic Navy
B.S., Naval Postgraduate School, 1979

Submitted in partial fulfillment of the requirements for the degree of

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ABSTRACT

Digital systems are of major importance in modern communications. This research investigates the minimum clock (bit) rate of a commercially available delta modulator/demodulator needed to transmit intelligible voice signals.

Intelligible voice and music signals were recovered using a clock rate as low as 6 Kbits/sec.

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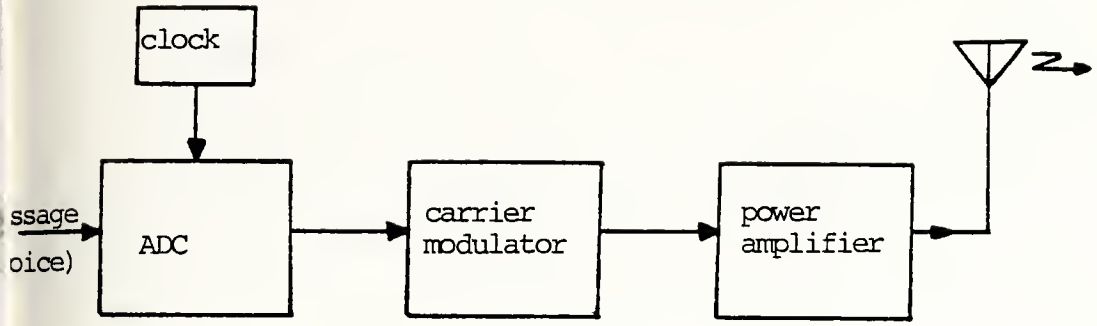
Table of Symbols and Abbreviations

$e(t)$	-	error waveform
$x(t)$	-	analog input to delta modulator
$\hat{x}(t)$	-	an approximation to $x(t)$
$y(t)$	-	delta modulator integrator output
$L(t)$	-	binary pulses from delta modulator
T	-	period of the clock waveform
$\pm V$	-	delta modulator step size
τ	-	pulse width
CVSD	-	continuously variable slope delta modulator
IC	-	integrated circuit
LPF	-	lowpass filter
ΔM	-	delta modulation

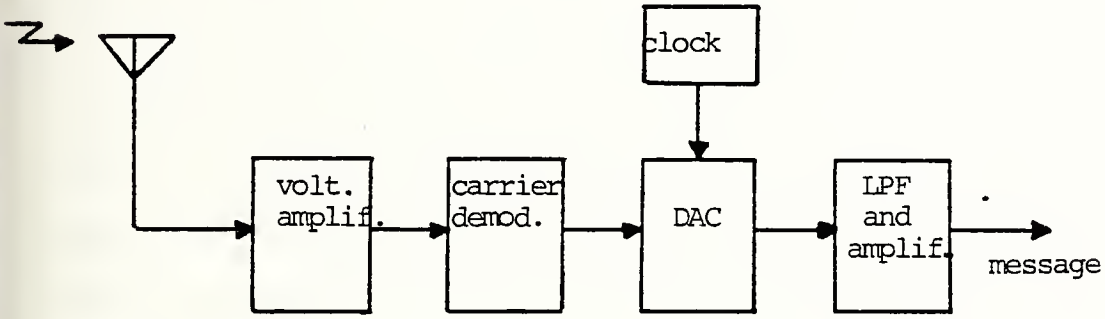
I. INTRODUCTION

Fig. 1 shows a block diagram of a typical digital communication system. This research considers the analog-to-digital conversion (ADC), and digital-to-analog conversion (DAC) subsystems when the message is a voice signal. For ADC in the transmitter, delta modulation is used.

The objective of this research is the determination (experimentally) of the minimum transmitter clock rate (bits per second) which will allow recovery of an intelligible voice signal in the receiver. A value of 6000 bits per second was found to be acceptable using the circuitry described in Chapter III of this report.



a. Transmitter



b. Receiver

Figure 1 Block Diagram of a Typical Communication System

II. BACKGROUND

A. DELTA MODULATION

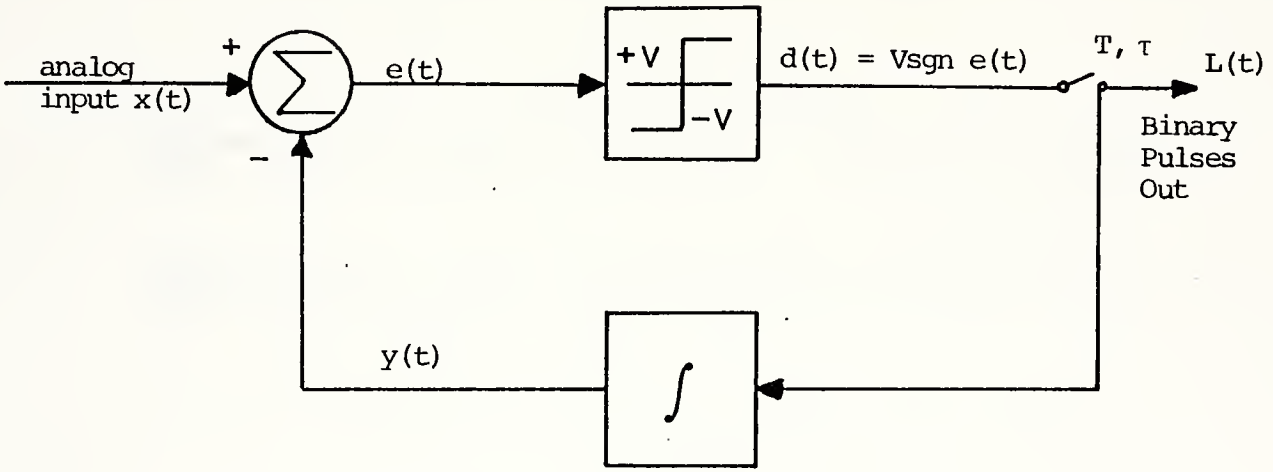
Delta Modulation (ΔM) is one of several methods of analog-to-digital conversion. The output of a delta modulator represents changes in signal amplitude from sampling instant to sampling instant. The schematic diagram of a basic ΔM system is shown in Fig. 2.

1. Encoder

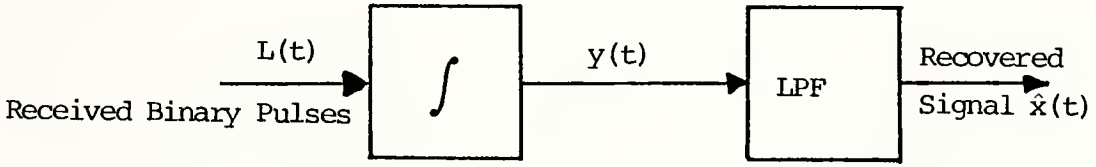
The basic encoder converts the applied band limited analog signal x(t) to pulses of fixed bipolar amplitude ($\pm V$ volts) and fixed duration (τ seconds). The pulses of the output L(t) are spaced T seconds apart ($T >> \tau$) as shown in Fig. 3. The clock rate of the output pulses is then $F_c = 1/T$. When the slope of the input signal x(t) is positive, the output waveform L(t) has more positive pulses than negative ones as explained below. The situation is reversed when x(t) has a negative slope as shown in Fig. 3. For a DC input L(t) consists of alternating positive and negative pulses.

In the encoder the output L(t) is integrated to form y(t). The difference between x(t) and y(t) is the error signal e(t). This error signal is quantized to levels $\pm V$ volts. This means the sign and not the magnitude of the error is preserved. The output of the quantizer is sampled every T seconds to form L(t).

If $e(t) \geq 0$ at a clock instant a positive pulse will be produced at the output of the encoder. When the pulse is



a. Encoder



b. Decoder

Figure 2. Basic ΔM System

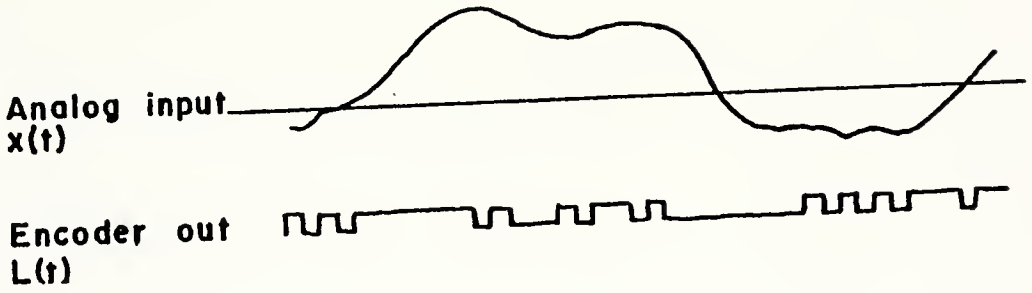


Figure 3. Analog Input and Encoder Output of Delta Modulator

integrated, y(t) is increased by a positive step. This increase in y(t) will be subtracted from x(t) and a change in the magnitude of the error signal occurs. If the error has not become negative by the next clock instant the output of the decoder will again be a positive pulse. As long as $e(t) \geq 0$, at successive clock instants a sequence of positive pulses will be produced. Eventually y(t) will become greater than x(t) at a clock instant and $e(t) < 0$ and a negative pulse will occur at the output of the encoder.

Thus the ΔM attempts to minimize the error e(t) by varying the polarity of the clocked pulses at the output of the encoder.

2. Decoder

The basic ΔM decoder consists of an integrator and a simple lowpass filter (LPF) as shown in Fig. 2(b). Assuming errorless transmission, the signal L(t) is recovered and integrated to give y(t) which is the same as the feedback signal in the encoder. Since y(t) differs from the input x(t) by a relatively small error signal e(t), it follows that the signal at the output of the integrator in the delta demodulator is a good reproduction of the original input signal. The step-like nature of y(t) is removed by passing this signal through a LPF.

Several problems in linear ΔM can be identified. Slope overload occurs when the analog input changes between samples by an amount greater than the step size ±V. This occurs if the input frequency or amplitude is too great.

There is also a minimum amplitude level that the ΔM can follow. If the peak to peak values are smaller than $|\pm V|$ the output will be as if x(t) were constant. Many methods of expanding the dynamic range and frequency response of ΔM have been explored [Ref. 2]. In this research a continuously variable slope (CVSD) modulation algorithm is used.

3. CVSD

In the CVSD modulator, circuitry external to the basic delta modulator monitors the past few outputs of the basic delta modulator in a simple three bit shift register. When all three bits in the shift register are "one's" or "zero's" it indicates that the gain of the integrator is too small. This condition results when the analog input voltage increases or decreases rapidly. At the slope polarity switch the step size magnitude increases (or decreases) at each clock pulse until the all "one's" (or all "zero's") condition no longer holds. Because the algorithm only operates on the past serial data, it changes the nature of the bit stream without changing the channel bit rate.

In the demodulator, the same algorithm and similar circuitry is used to monitor the sequence of "one's" and "zero's" and change the gain of the integrator in an appropriate manner.

B. SPEECH CHARACTERISTICS

Significant frequency components of human voice are concentrated in the range from 300 to 3000 Hz. This band of

frequencies is transmitted by commercial telephone systems, for example.

For commercial digital communication systems using pulse code modulation (PCM), 8000 samples per second and 8 bits per sample are used for a bit rate of 64 kilobits per second.

For commercial telephone systems using CVSD ΔM, 32 kilobits per second is a recommended rate.

III. HARDWARE IMPLEMENTATION

A. OVERALL SYSTEM

The system used in this research consists of two major parts, the transmitter section and the receiver section.

Fig. 4 is the block diagram of the transmitter and wave forms at various nodes. Fig. 5 shows the block diagram of the receiver and wave forms at various nodes.

In the transmitter, an audio amplifier provides a proper level of the voltage form of the human speech signal. This analog message voltage is converted to digital form by a delta modulator. This digital signal is then applied to a delta demodulator (digital to analog converter) in the receiver. The analog voltage is lowpass filtered and amplified by an audio amplifier which drives a speaker.

In this implementation the delta modulator and demodulator are connected to the same clock. In this way, the synchronization problem is avoided.

B. TRANSMITTER SUBSYSTEM

1. Voice Source

A male speaker's voice signal is recorded on a tape recorder which upon playback provides a repeatable message voltage.

2. Audio Amplifier

The audio amplifier uses a LM-380 integrated circuit (I.C.) to provide 34 db of gain. Circuit connections are shown in Fig. 10 of the Appendix.

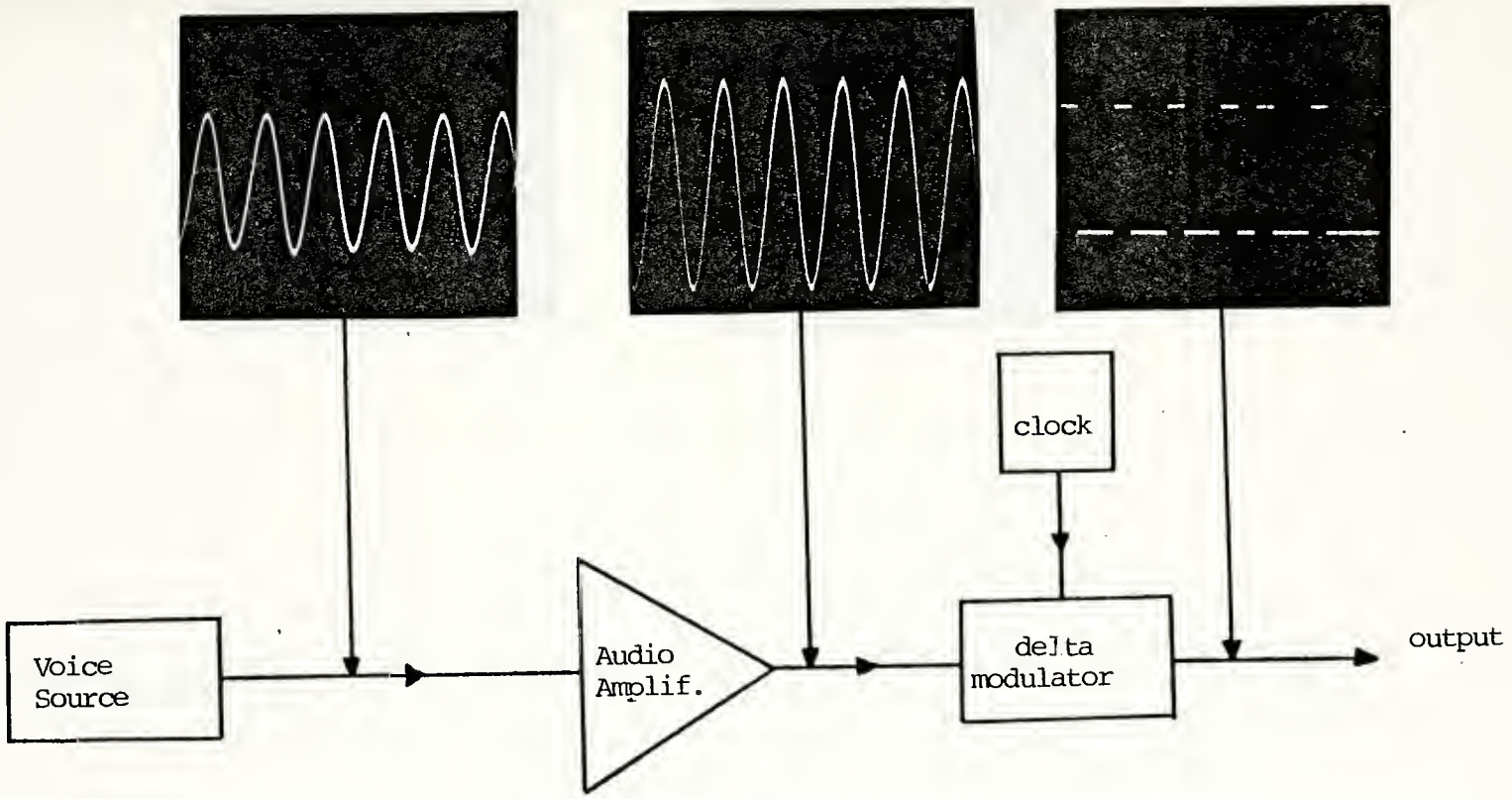


Figure 4. Transmitter Block Diagram

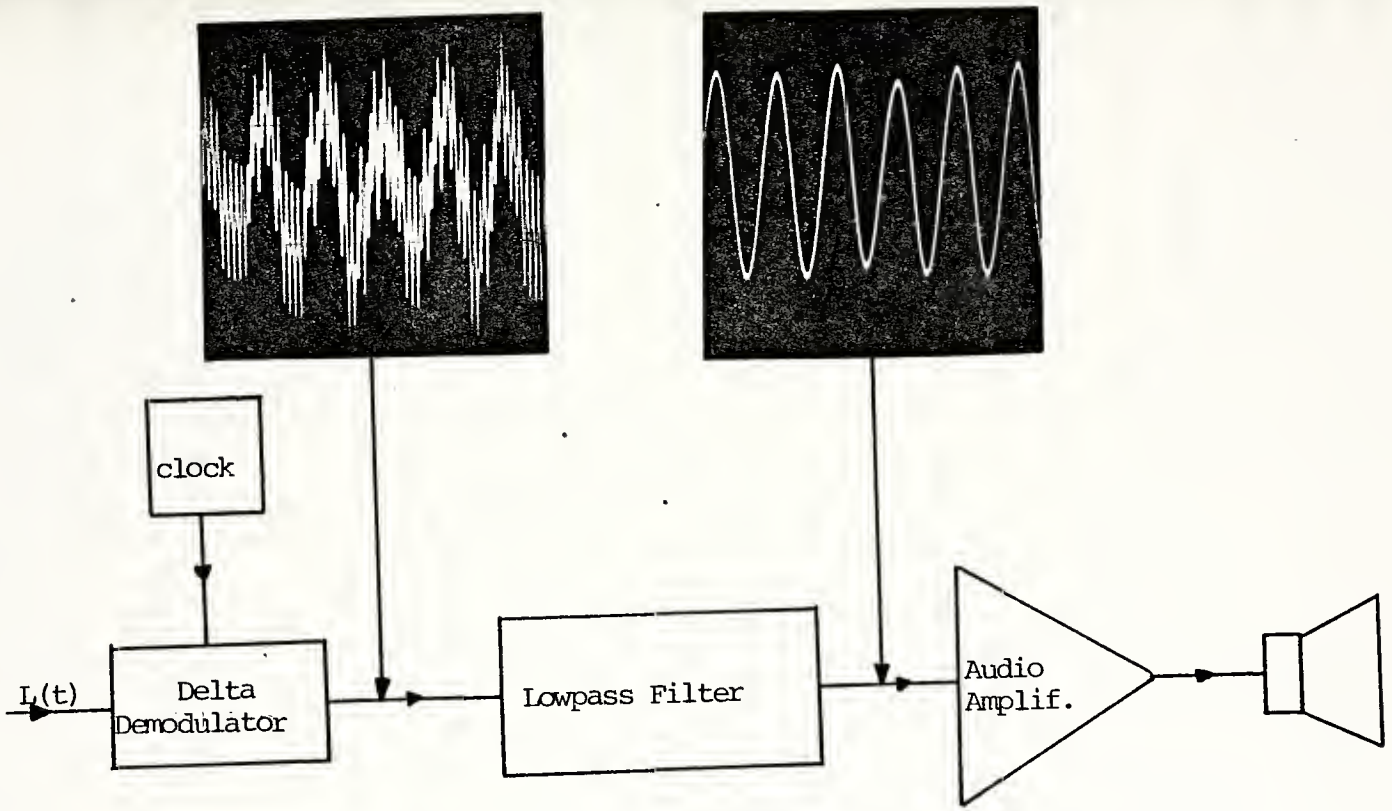


Figure 5. Receiver Block Diagram

3. Delta Modulator

The delta modulator uses a Motorola MC-3417L IC codec (encoder-decoder). Rather than providing bipolar pulses the output of this IC is a plus voltage for data "one" and ground for data "zero" which is compatible with TTL integrated circuits.

The delta modulator consists of a comparator in the forward path of a simple control loop as shown in Fig. 6. The input to the comparator is the difference between the input analog signal (human voice) and the integrator output of the delta modulator. The comparator output reflects the sign of its input voltage. That sign bit is the delta demodulator output, but it also controls the direction of the ramp in the output of the feedback integrator. The comparator is clocked to produce a synchronous and band limited digital bit stream. A sample and hold network following the voltage comparator provides the output pulses of duration T (the clock period).

The schematic diagram of the CVSD modulator is contained in the Appendix.

C. RECEIVER SUBSYSTEM

1. Delta Demodulator

The delta demodulator uses the same IC as the delta modulator (Motorola MC-3417L).

The delta demodulator consists of a sampler, an integrator and continuously variable slope system as shown in Fig. 7.

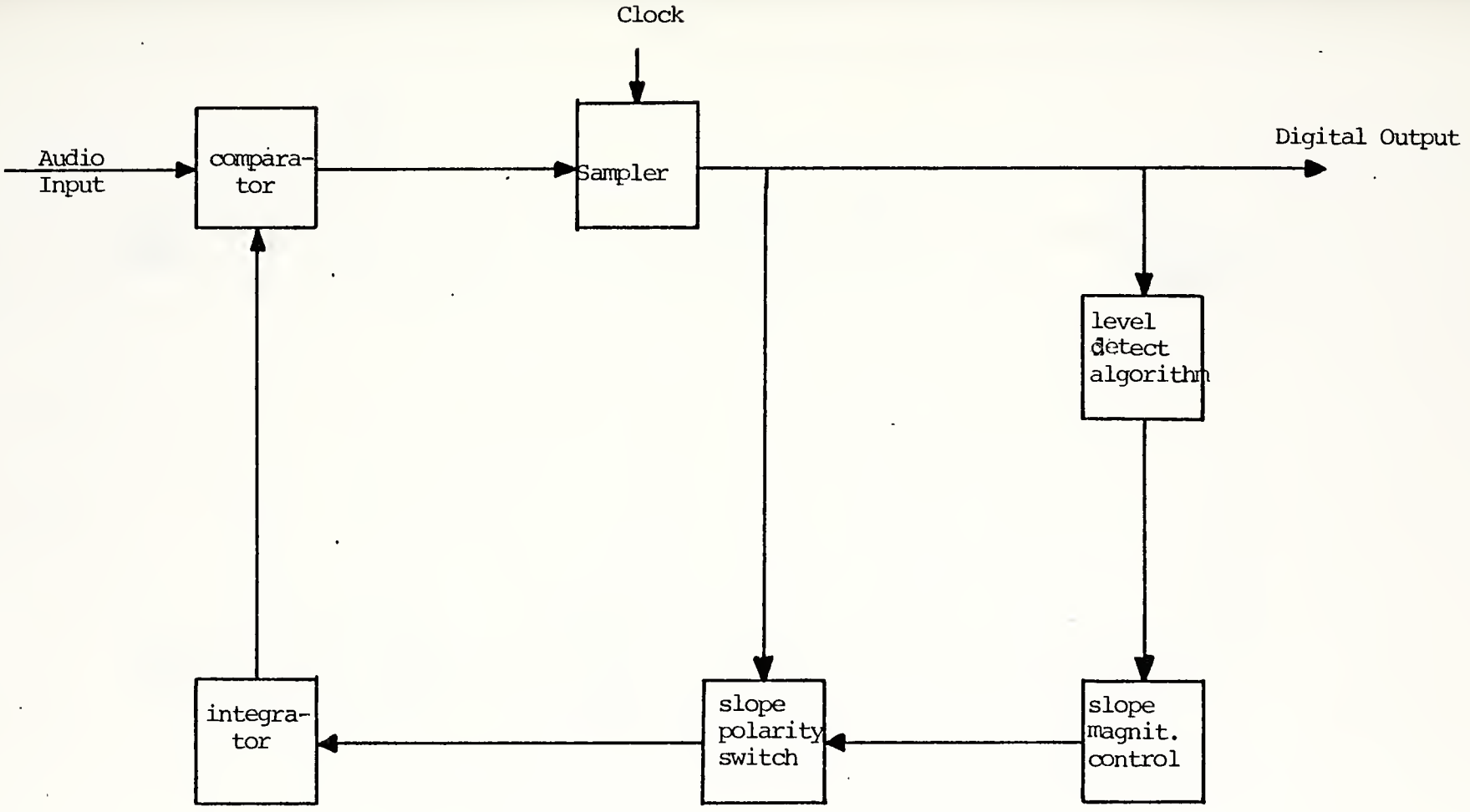


Figure 6. Block Diagram of the MC 3417 Modulator

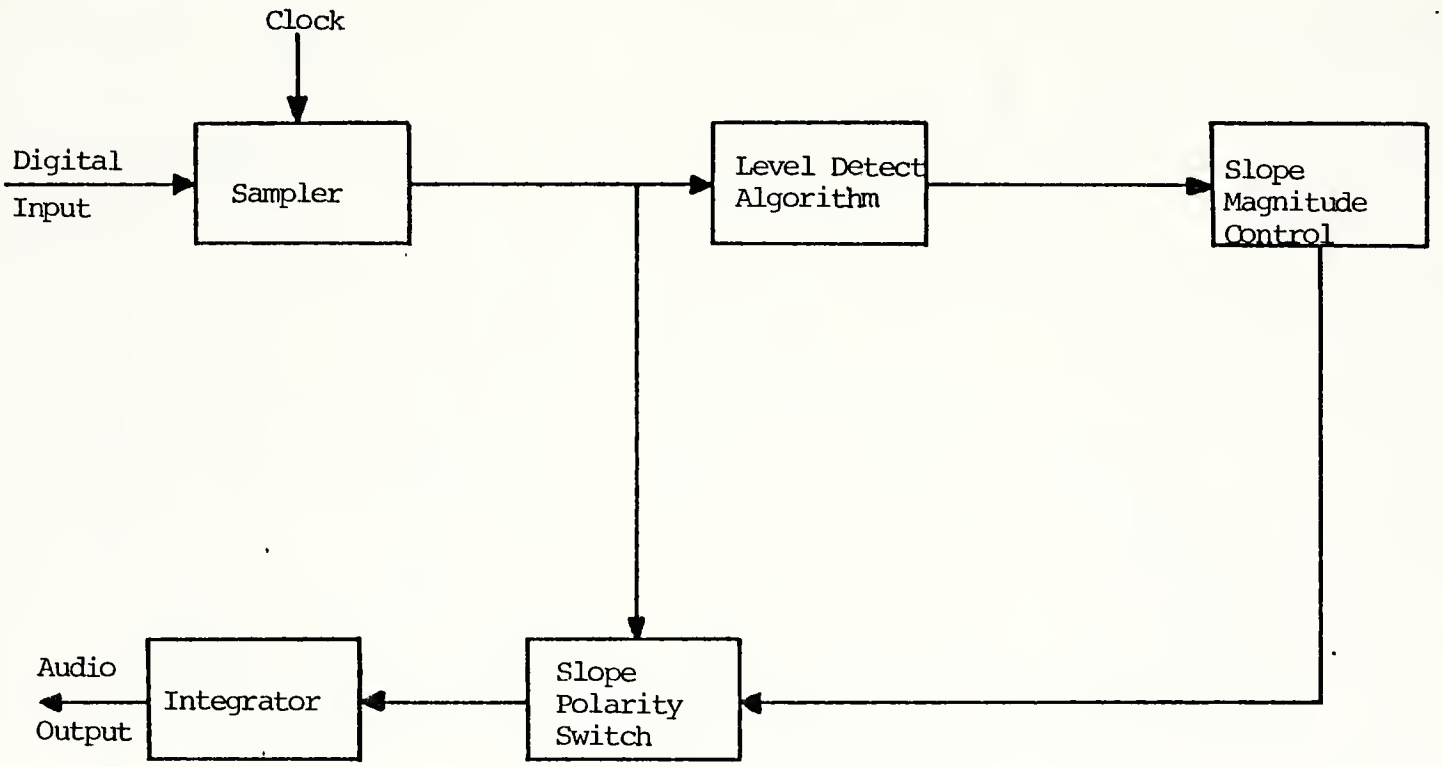


Figure 7. Block Diagram of the MC 3417 Demodulator

The digital signal in the receiver is integrated by the delta demodulator to provide the analog output. The delta demodulator uses the same CVSD algorithm as the delta modulator. The analog output of the delta demodulator is also lowpass filtered.

Fig. 8 shows an example of waveforms associated with the CVSD IC. The filter output $\hat{x}(t)$ is an approximation to the original input $x(t)$. The Appendix contains the schematic diagram of the delta demodulator.

2. Lowpass Filter

Since the goal of this research is to determine the maximum clock rate which allows recovery in the receiver of an intelligible voice signal, several techniques were explored. The best results were given when the lowpass filter described in the Appendix was used in the output of the delta demodulator.

The LPF consists of two cascaded LPF's, each having a cutoff frequency of about 900 Hz. Each filter section is a six pole active LPF with three second order stages. The active device for each stage is a 741 IC operational amplifier. The transfer function of the LPF is given in the Appendix. Fig. 9 shows the measured frequency response of the LPF. The theory and performance are in good agreement.

The following techniques led to the choice of this LPF.

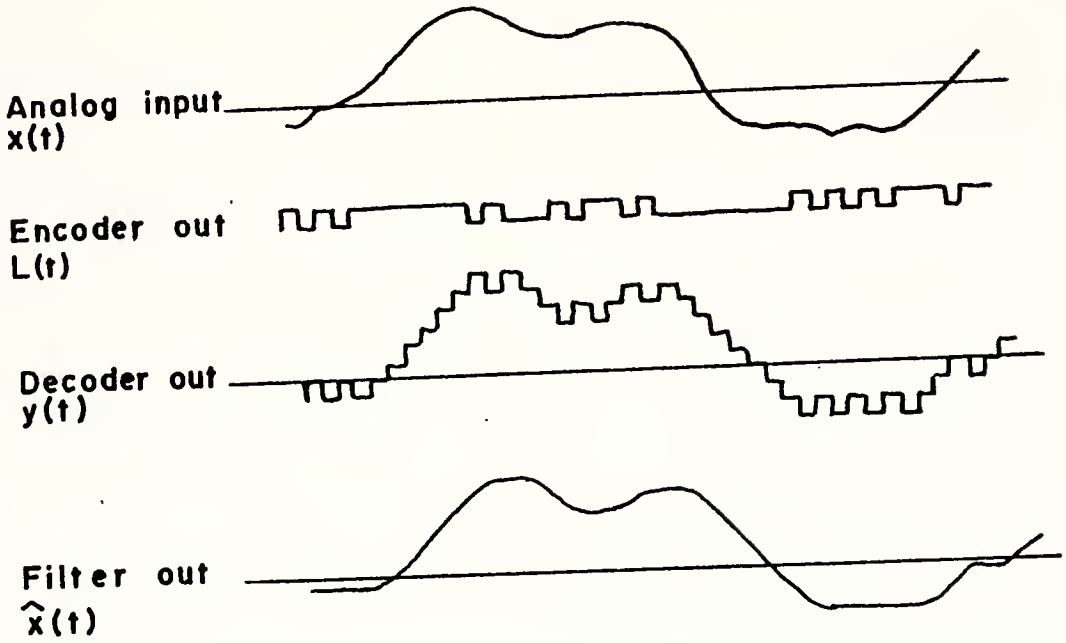


Figure 8. Example of Waveform Associated with the MC 3417 IC

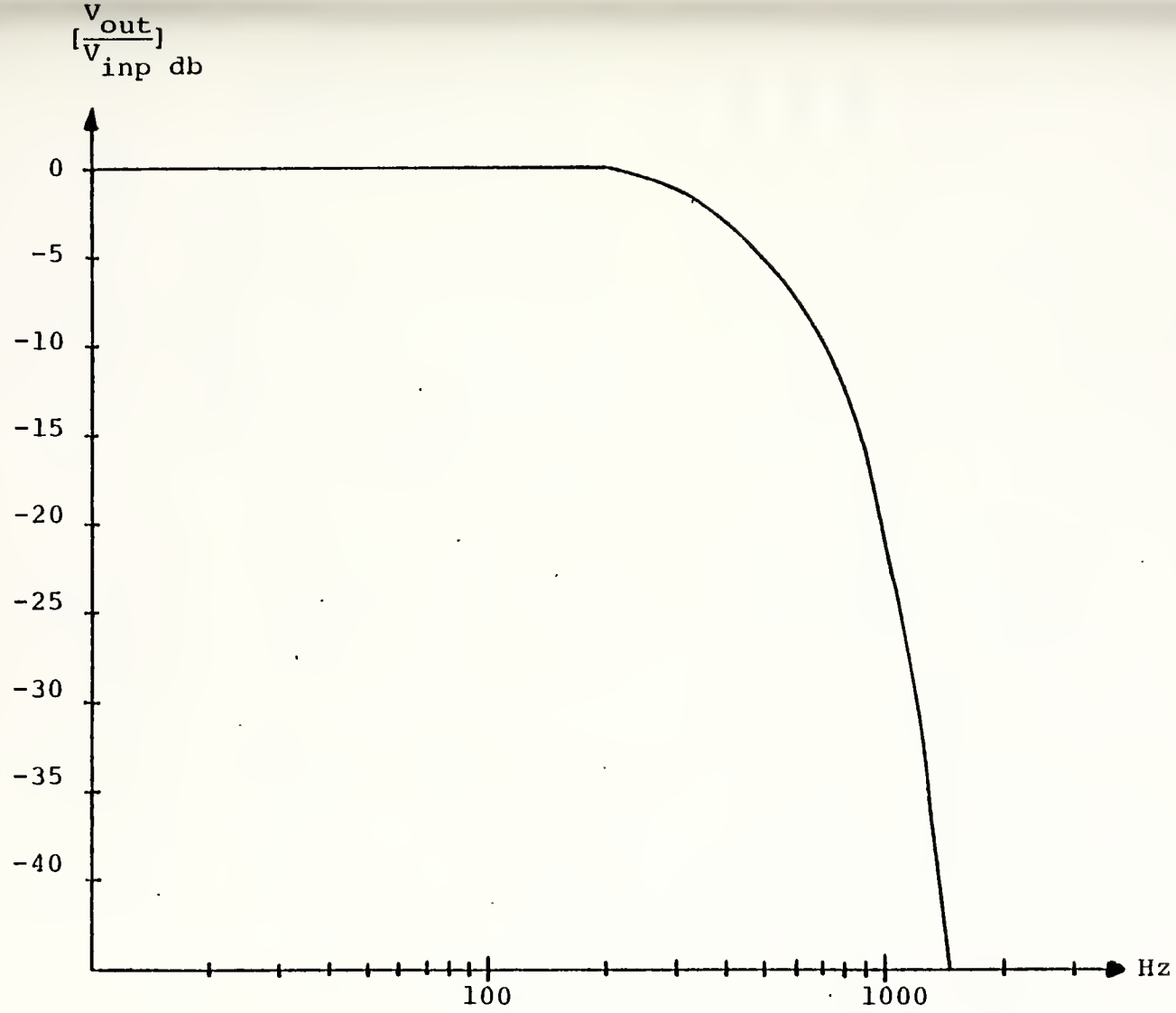


Figure 9. Measured Frequency Response of the LPF

a. The LPF as shown in Fig. 13 of the Appendix was used in the transmitter after the audio amplifier and before the delta modulator to reject voice frequency terms above 900 Hz. The output of the delta demodulator was filtered by filter No. 2 shown also in Fig. 13. To recover good quality voice in the receiver using this configuration, a clock rate of 8000 Hz is required.

b. The same configuration as in paragraph (a) was used but a differentiator was added after the LPF in the receiver. The problem with this configuration is that the high frequency components of noise as well as those of the signal are accentuated by the differentiator. Further, noise components having frequencies higher than those in the voice signal are emphasized and contribute to distortion in the output.

c. The same configuration as in paragraph (a) was used but a hard limiter and a LPF with a cut-off frequency of 3000 Hz were added after the LPF in the receiver. With the hard limiter, distortion of the voice signal occurred in the output of the receiver. The intent was to use the hard limiter to restore to the voice signal the high frequency components which were filtered in the transmitter.

3. Audio Amplifier

The receiver audio amplifier, used to drive the speaker is identical to that of the transmitter (Fig. 10).

4. Speaker

An 8Ω, 6 in by 6 in speaker is used.

IV. COMMENTS AND CONCLUSIONS

ΔM provides a relatively simple modulation/demodulation scheme. A single ΔM (Motorola MC-3417) IC provides A/D and D/A conversion for voice signals.

To recover in the receiver good quality human voice a clock rate of 6000 Hz is required with the system used in this research.

The input analog waveform need not be frequency limited to allow a reduction in the ΔM clock rate.

A lowpass filter in the receiver is needed to remove the audible clock frequency.

To further reduce the system clock rate without sacrificing signal quality, the following are suggested.

(1) A digital filter with uniform gain in the frequency range of the voice signal and great attenuation at the ΔM clock frequency can be used in the receiver to remove the interfering audible clock frequency.

(2) Consider other techniques which might be used to recover the high frequency components of the voice signal without interference from the clock signal. Possible techniques might include operating the receiver clock at a rate n times that of the transmitter where n is a positive integer > 1.

APPENDIX

Schematic Diagrams

The system used in this research consists of a transmitter section and receiver section. This Appendix presents and describes the schematic diagrams used in the final configuration of the transmitter and receiver portion of the system.

A. TRANSMITTER SUBSYSTEM

The transmitter subsystem consists of an audio amplifier and a delta modulator.

1. Audio Amplifier

The audio amplifier uses a LM 380 IC to provide about 34 db of gain when connected as shown in Fig. 10.

The input connection of the LM 380 op-amp allows the applied signal to be referenced to ground (zero volts).

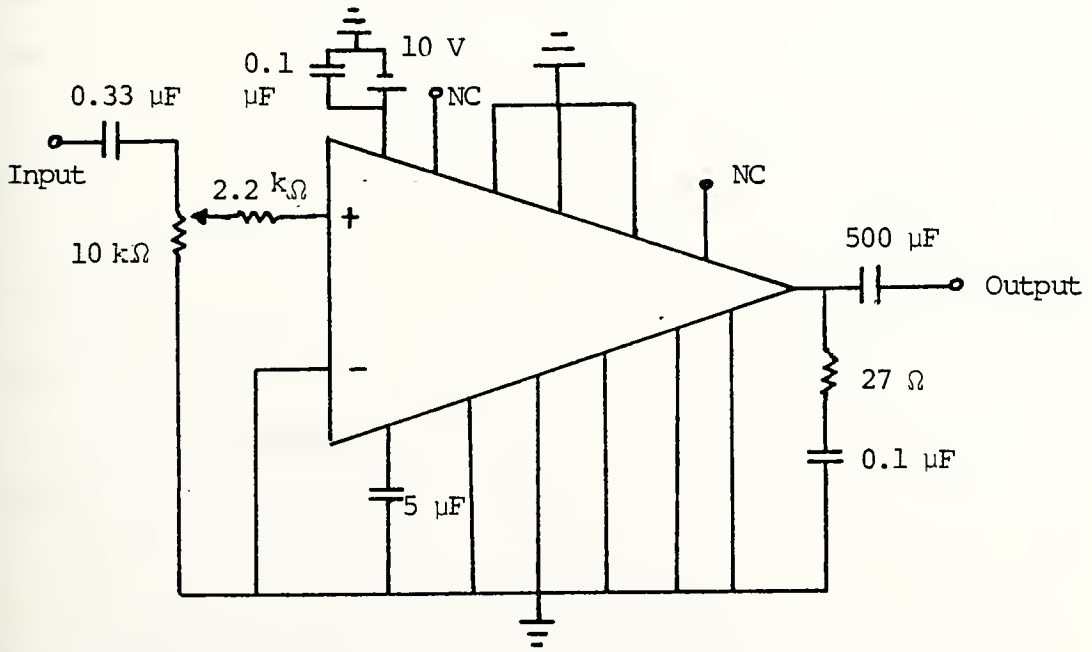


Figure 10. Schematic Diagram of the Audio Amplifier

2. Delta Modulator

The delta modulator uses a Motorola MC-3417 IC connected as shown in Fig. 11.

A model 136 WAVETEK function generator provides a variable frequency clock (square wave output).

B. RECEIVER SUBSYSTEM

The receiver subsystem consists of a delta demodulator, a lowpass filter, an audio amplifier and a speaker.

1. Delta Demodulator

The delta demodulator uses a Motorola MC-3417L IC connected as shown in Fig. 12. It uses the same clock as the delta modulator.

2. Lowpass Filter

A lowpass filter with a cut-off frequency of 1 kHz was built using two cascaded 6^{th} order lowpass filters (No. 1 and No. 2) with active elements as shown in Fig. 13. See Reference 3 for the design procedure.

Each LPF section consists of three second order stages. Each second order stage is (Fig. 14) of the voltage controlled voltage source (VCVS) or an equal component value Sallen-key type [Ref. 4]. The active device for each stage is a 741 operational amplifier.

The transfer function of each second order stage (refer to Fig. 14) is:

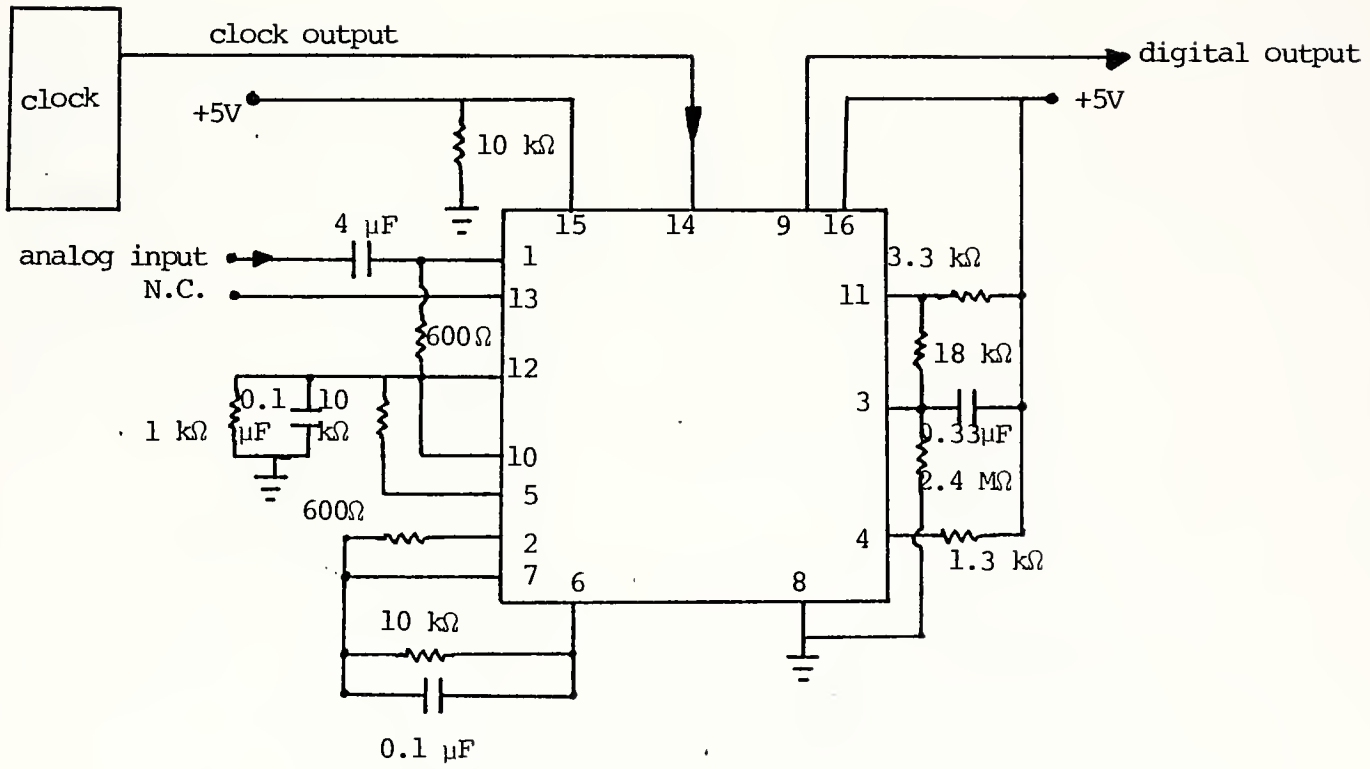


Figure 11. Schematic Diagram of Delta Modulator

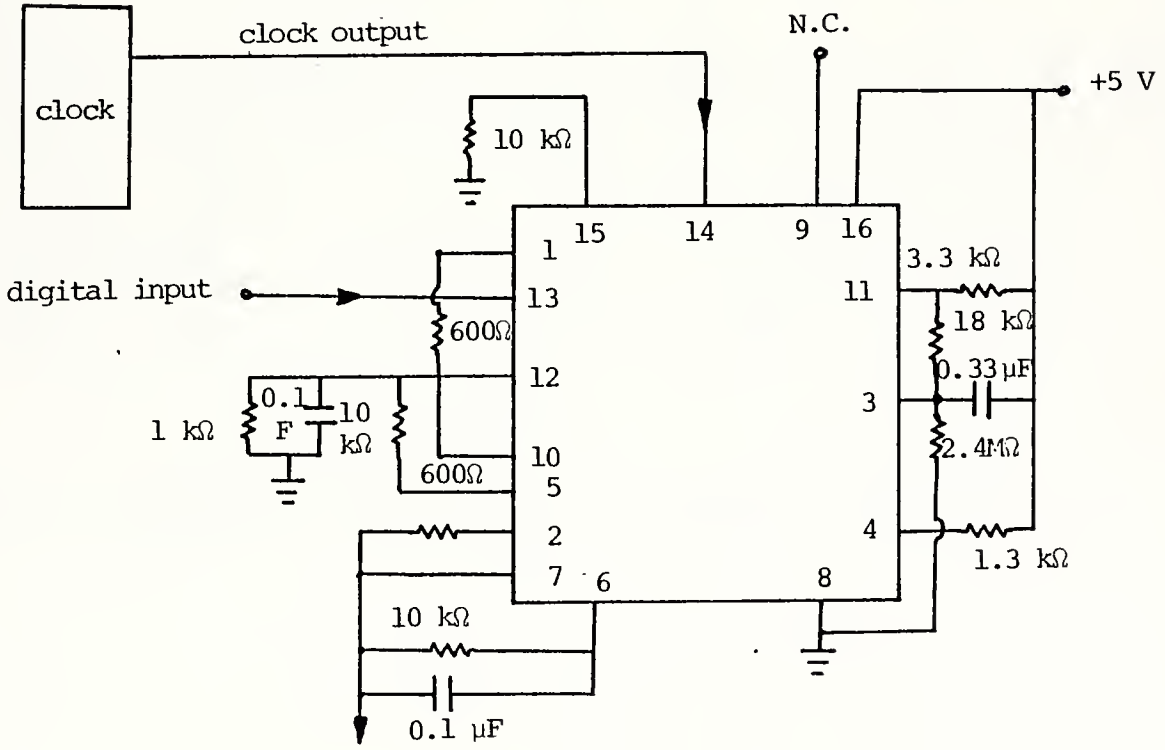


Figure 12. Schematic Diagram of Delta Demodulator

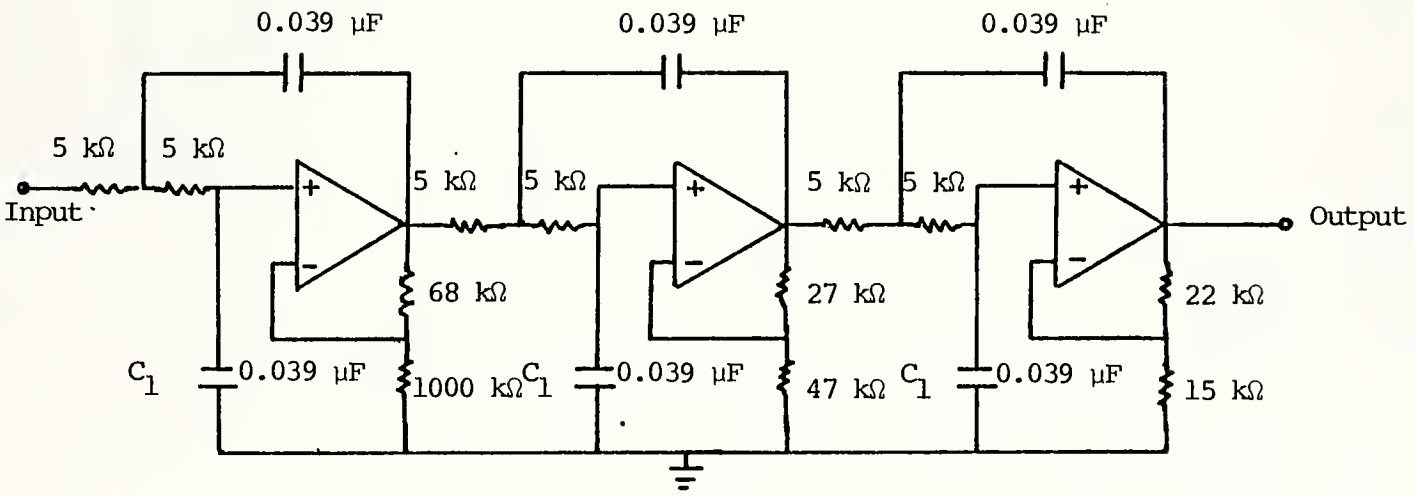


Figure 13. Schematic Diagram of No. 1 Lowpass Filter, in Lowpass Filter No. 2, C_1 = 0.033 μF

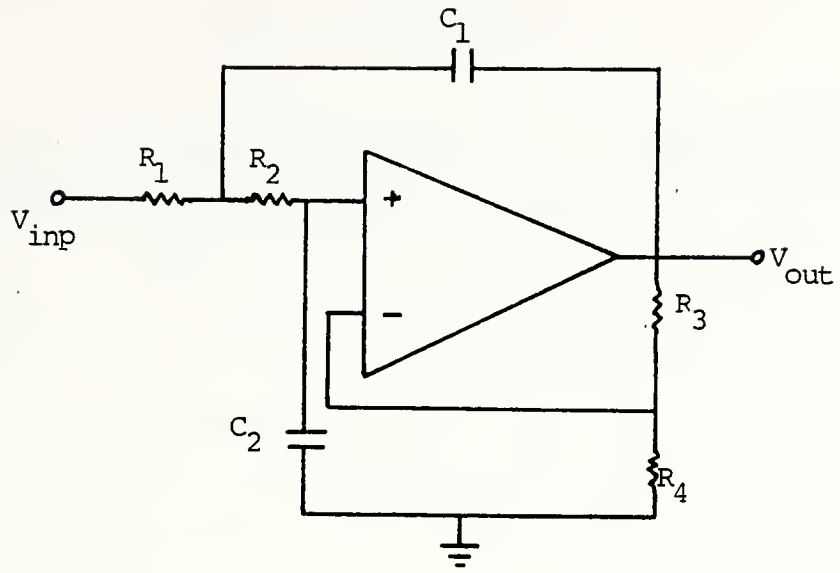


Figure 14. One Stage Second Order of the Lowpass Filter

$$\frac{V_{out}}{V_{inp}} = \frac{\frac{K}{R_1C_1R_2C_2}}{S^2 + [\frac{1}{R_2C_1} + \frac{1}{R_1C_1} + (1-K)\frac{1}{R_2C_2}]S + \frac{1}{R_1R_2C_1C_2}}$$

where K is the gain of the stage.

In the Salley-key circuit the gain is given by:

$$K = 1 + \frac{R_3}{R_4} .$$

3. Audio Amplifier

The receiver audio amplifier is identical to that in the transmitter (Fig. 10).

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3. Lancaster, D., Active Filter Cookbook, H.W. Sams and Co., 1975.

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